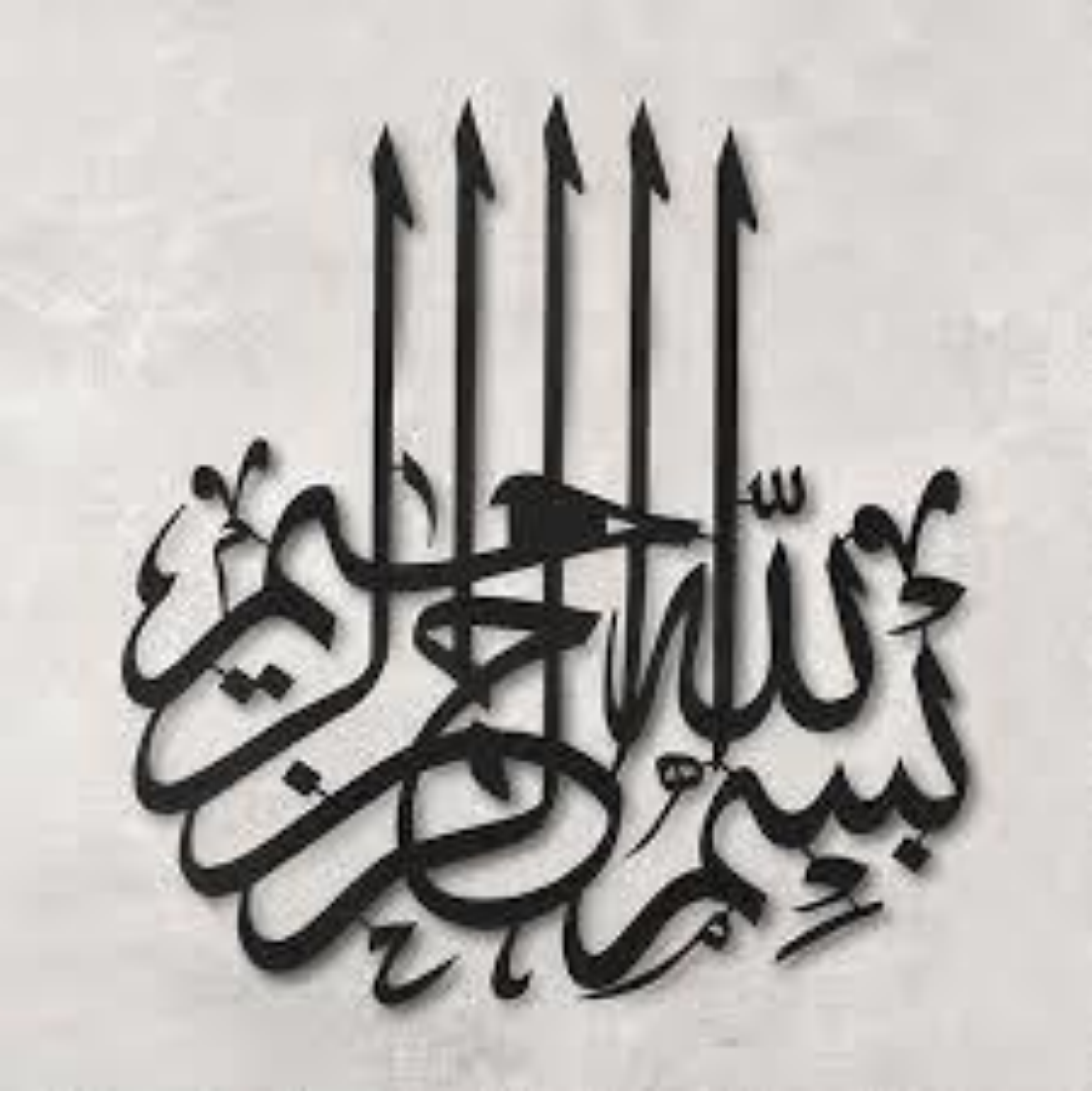
بسم الله الرحمن الرحيم

CHAPTER

3

p–n Junction

3.5 CHARGE STORAGE AND TRANSIENT BEHAVIOR

- Under forward bias, electrons are injected from the n-region into the p-region and holes are injected from the p-region into the n-region.

- Once injected across the junction, the minority carriers recombine with the majority carriers and decay exponentially with distance, as shown in Fig. 15a.

- These minority-carrier distributions lead to current flow and to charge storage in the *p–n* junction.

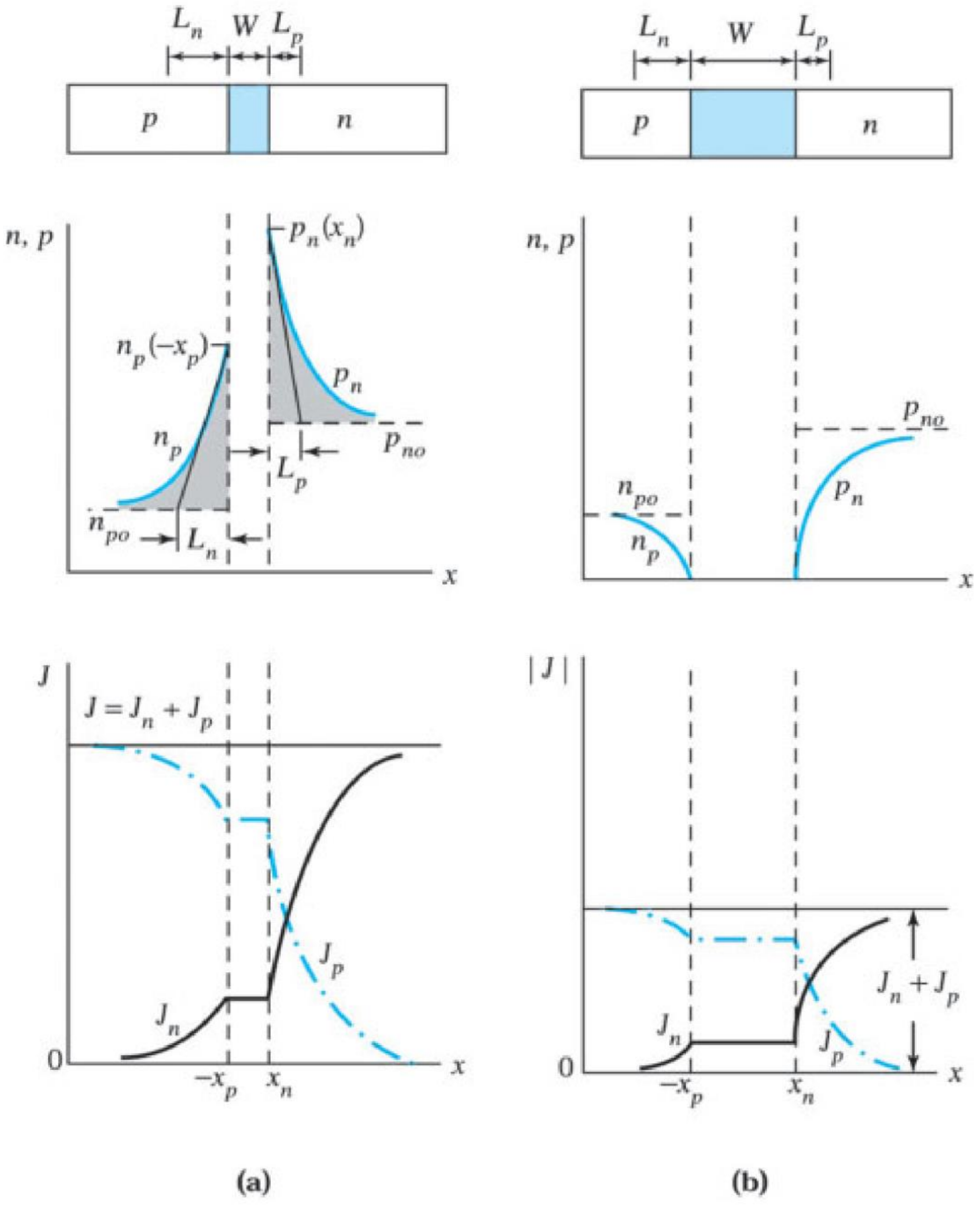

Fig. 15 Injected minority carrier distribution and electron and hole currents. (*a*) Forward bias. (*b*) Reverse bias. The figure illustrates idealized currents. In practical devices, the currents are not constant across the space charge layer.

- We consider the stored charge, its effect on junction capacitance, and the transient behavior of the p–n junction due to sudden changes of bias.

3.5.1 Minority-Carrier Storage

- The charge of injected minority carriers per unit area stored in the neutral *n*-region can be found by integrating the excess holes in the neutral region, shown as the shaded area in the middle of Fig. 15*a*, using Eq. 51:

$$p_n - p_{no} = p_{no}\left(e^{qV/kT} - 1\right)e^{-(x-x_n)/L_p}, \qquad (51)$$

$$
\begin{aligned}
Q_p &= q\int_{x_n}^{\infty}(p_n - p_{no})\,dx \\
&= q\int_{x_n}^{\infty} p_{no}\left(e^{qV/kT} - 1\right) e^{(x-x_n)/L_p}\,dx \\
&= qL_p p_{no}\left(e^{qV/kT} - 1\right).
\end{aligned}
\qquad (75)
$$

L_p is the average distance of a hole diffusion before recombining.

- The stored charge can be regarded as the hole diffusion with an average distance of L_p away from the boundary of the depletion region.

- The number of stored minority carriers depends on both the diffusion length and the charge density at the boundary of the depletion region.

- A similar expression can be obtained for the stored electrons in the neutral *p*-region.

- We can express the stored charge in terms of the injected current.

- From Eqs. 52 and 75, we have

$$J_p(x_n) = -qD_p \left.\frac{dp_n}{dx}\right|_{x_n} = \frac{qD_p p_{no}}{L_p}\left(e^{qV/kT} - 1\right). \tag{52}$$

$$Q_p = \frac{L_p^{\ 2}}{D_p} J_p(x_n) = \tau_p J_p(x_n). \qquad (76)$$

The average lifetime of holes in n-side is τ_p.

- Thus, the stored charges Q_p must be replenished(دوباره پر شدن) every τ_p seconds.

بعبارتی بعد از گذشت طول عمر حفره، حفره های دیگری باید از P به N دیفیوژ می شوند تا فرآیند تداوم جریان برقرار باشد

- Equation 76 states that the amount of stored charge depends on the current and lifetime of the minority carriers.

EXAMPLE 7

For an ideal abrupt silicon p^+–n junction with $N_D = 8 \times 10^{15}$ cm^{-3}, calculate the stored minority carriers per <u>unit area</u> in the neutral n-region when a forward bias of *1V* is applied. The diffusion length of the holes is 5 µm.(T=300K)

$$Q_p = qL_p p_{no}\left(e^{qV/kT} - 1\right). \qquad (75)$$

$$p_{po} n_{po} = n_i^2 \qquad p_{no}\, n_{no} = n_i^2$$

$$n_i = 9.65 \times 10^9$$

$$n_{no} = N_D \qquad p_{po} = N_A$$

3.5.2 Diffusion Capacitance

- The depletion-layer capacitance considered previously accounts for most of the junction capacitance when the junction is reverse biased.

- When the junction is forward biased, there is an additional significant contribution to junction capacitance from the rearrangement of the stored charges in the neutral regions.

- This is called the *diffusion capacitance*, denoted C_d, a term derived from the ideal-diode case in which minority carriers move across the neutral region by diffusion.

- The diffusion capacitance of the stored holes in the neutral n-region is obtained by applying the definition

$C_d \equiv AdQ_p/dV$ to Eq. 75:

در واقع این همان تعریف عمومی ظرفیت است و dQ به این خاطر در A ضرب شده است که dQ بار واحد سطح است.

$$C_d = \frac{Aq^2 L_p p_{no}}{kT} e^{qV/kT}, \tag{77}$$

where A is the device cross-section area.

- We may add the contribution to C_d of the stored electrons in the neutral p-region in cases of significant storage.

- For a p^+–n junction, however, $n_{po} << p_{no}$, and the contribution to C_d of the stored electrons becomes insignificant. توضیح در اسلاید بعدی

- Under reverse bias (i.e., V is negative), Eq. 77 shows that C_d is inconsequential (بی اهمیت)because of negligible minority-carrier storage.

- In many applications we prefer to represent a p–n junction by an equivalent circuit.

- In addition to diffusion capacitance C_d and depletion capacitance C_j, we must include conductance to account for the current through the device.

- In the ideal diode the conductance can be obtained from Eq. 55:

جلسه ۲۰

①

در حالت پیوند $p^+ - n$ یعنی ($N_A >> N_D$) یا ($p_{p_0} >> n_{n_0}$)

از طرفی بنا به قانون:

$$\begin{cases} p_{p_0} n_{p_0} = n_i^2 \\ \Rightarrow p_{p_0} = \frac{n_i^2}{n_{p_0}} \quad ② \end{cases} \quad \text{و} \quad \begin{cases} p_{n_0} n_{n_0} = n_i^2 \\ n_{n_0} = \frac{n_i^2}{p_{n_0}} \quad ③ \end{cases}$$

$$(1, 2, 3) \Longrightarrow \frac{n_i^2}{n_{p_0}} >> \frac{n_i^2}{p_{n_0}} \Longrightarrow p_{n_0} >> n_{p_0}$$

بدون اثبات فوق هم می‌توان رابطه فوق را فهمید زیرا در پیوند $p^+ - n$ چون چگالی حفره‌ها در P از چگالی الکترونها در N خیلی بیشتر است منطقی است که بدلیل تعداد زیاد حفره‌ها در طرف P حاملهای اقلیت یعنی الکترونها (n_{p_0}) بدلیل احتمال بازترکیب با حفره‌ها کاهش یابد. این کاهش در مقایسه با کاهش حفره‌ها در طرف N که تعداد الکترونها در آنجا خیلی زیاد نیست، خیلی زیاد است

$$J = J_p(x_n) + J_n(-x_p) = J_s\left(e^{qV/kT} - 1\right), \quad (55)$$

$$G = \frac{AdJ}{dV} = \frac{qA}{kT} J_s e^{qV/kT} = \frac{qA}{kT}(J + J_s) \cong \frac{qI}{kT} \quad . \quad (78)$$

در واقع AdJ همان dI هستش و جریان بر ولتاژ، معکوس مقاومت یا همان رسانش است. قسمت ماقبل آخر را از رابطه ۵۵ بدست آورده یعنی J_s را به داخل پرانتز ضرب کرده و حاصلضرب J_s در جمله نمایی را برابر J_s +J نوشته است.

- The diode equivalent circuit is shown in Fig. 19, where C_j stands for the total depletion capacitance (i.e., the result in Eq. 33 times the device area A).

چون رابطه زیر برای واحد سطح بدست آمده است باید در A ضرب شود

$$C_j = \frac{\varepsilon_s}{W} \quad \text{F/cm}^2. \quad (33a)$$

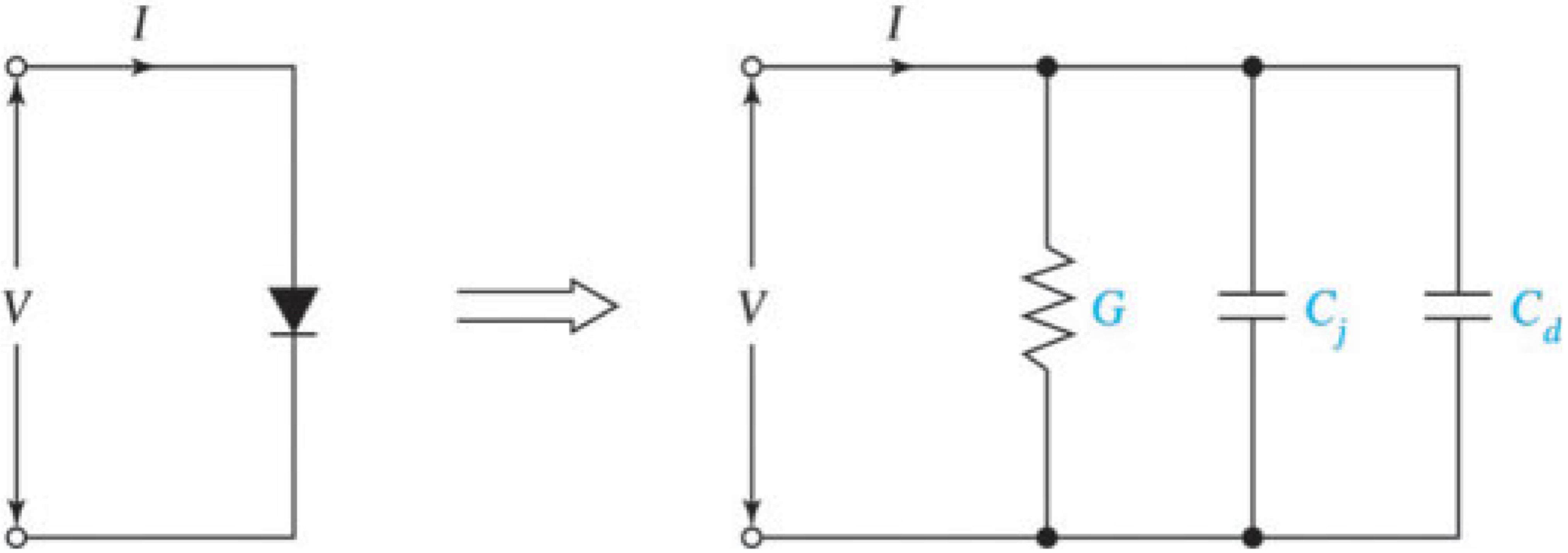

Fig. 19 Small-signal equivalent circuit of a *p–n* junction.

- For low-voltage, sinusoidal excitation of a diode that is biased quiescently(آرام) (i.e.,at dc), the circuit shown in Fig. 19 provides adequate accuracy.

- Therefore, we refer to it as the diode small-signal equivalent circuit.